FACILITATING ANALYSIS AND SYNTHESIS TECHNOLOGIES FOR EFFECTIVE RECONFIGURATION

Key Innovation

Motivation

- Creation of reconfigurable systems is not straightforward
- The designer has to
  - Identify the portions to be reconfigured
  - Establish a schedule that (a) respects dependencies, while at the same time (b) performs well and (c) meets constraints such as power, area and reconfiguration time
  - Manage the system resources (mainly reconfigurable area)
  - Verify a **changing** system
- Tool support for these tasks is esoteric to say the least
- Resource management is up to the user
- Verification: is it even possible?

Goals

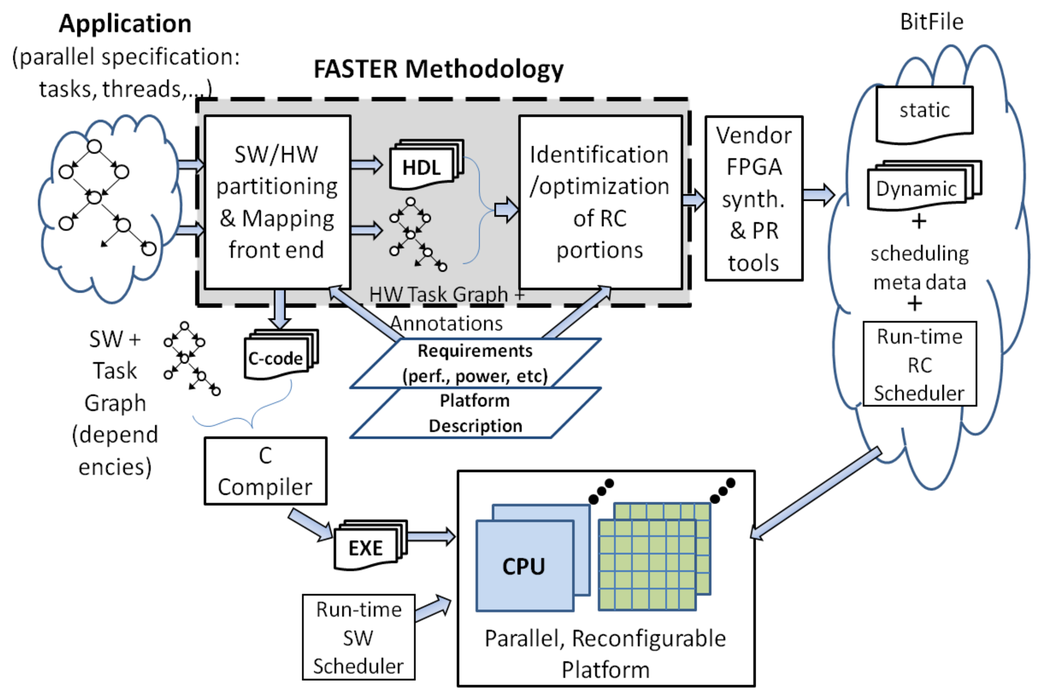
FASTER project addresses the above by:

- Including **reconfigurability as an explicit design concept** in computing systems design, along with **methods and tools** that support run-time reconfiguration in the entire design methodology
- Providing a framework for analysis, synthesis and verification of a reconfigurable system
- Providing efficient and transparent runtime support for partial and dynamic reconfiguration, including micro-reconfiguration
- Demonstrating usability and performance on commercial applications offered by the industrial partners

Technical approach

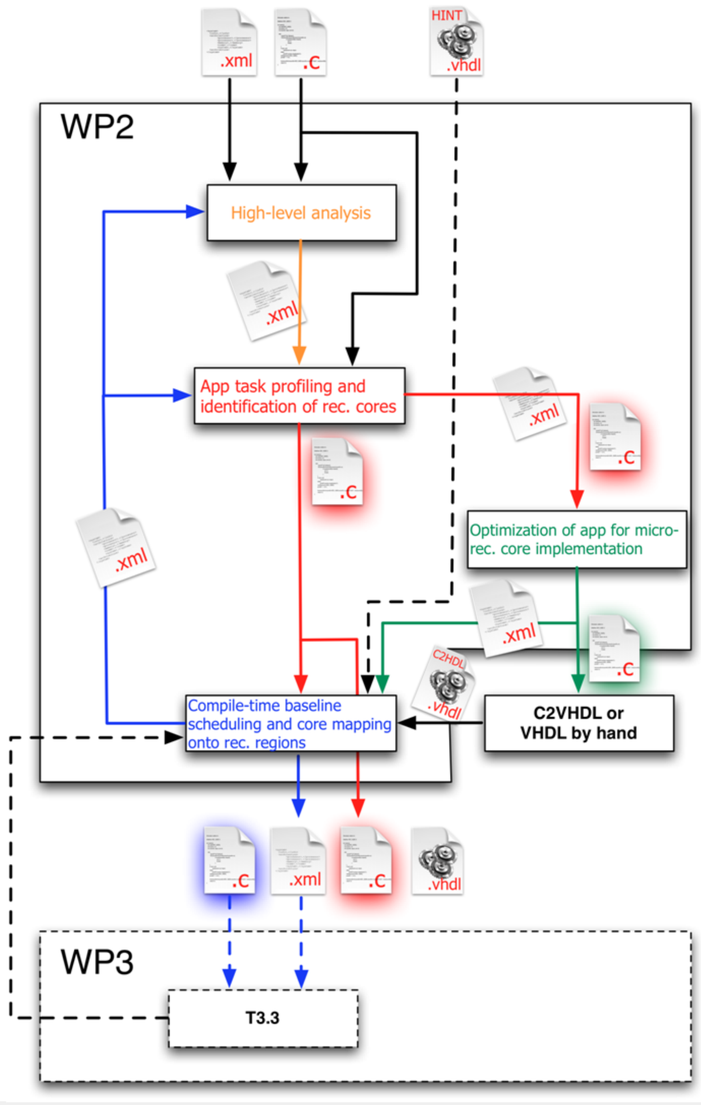
Novel tool-chain allowing to

- Define the application components categorized in
  - Static HW part, reconfigurable HW modules, software part
- Provide an analytical model of a reconfigurable design
  - By relating application attributes with possible implementation parameters
  - By estimating metrics (speed, area, power)
- Estimate, identify and optimize performance and constraints on the target reconfigurable system
  - Execution time
  - Floorplanning/placement
  - HW/SW execution
  - Reconfiguration time



Realized by identifying

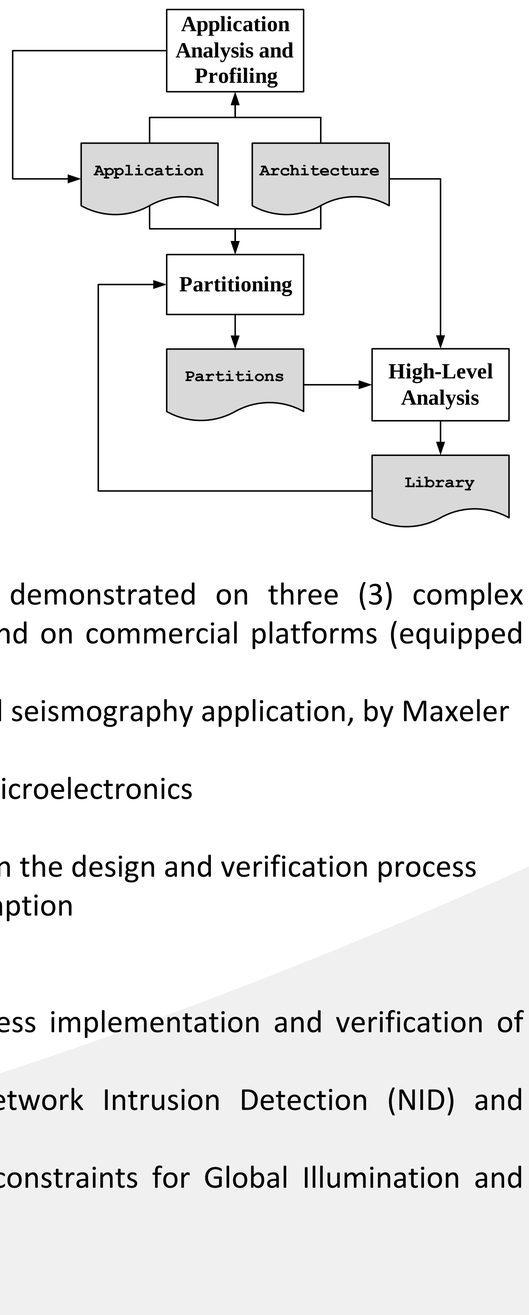
- Partitioning of the input specification in HW/SW components
- Implementation(s) of the modules to be realized as HW accelerators
- Corresponding level of reconfigurability for HW components, i.e. none, region-based, micro
- Power constraints
- Floorplanning constraints (size and shape)
- Placement requirements
- A baseline schedule for application execution



Methodology overview

Base procedure

- System described in XML format
- Four independent XML parts are analyzed, generated and updated
- Starting point is a C-like representation of the application
- A corresponding task graph is derived where every task is treated as region-reconfigurable or micro-reconfigurable module



Demonstration and use

- Effectiveness of the FASTER tool-chain will be demonstrated on three (3) complex applications from different application domains and on commercial platforms (equipped with Xilinx Virtex-6 FPGAs) :
  - Reverse Time Migration (RTM), a computational seismography application, by Maxeler Technologies
  - Global Illumination and Image Analysis, by ST Microelectronics
  - Netwok Intrusion Detection, by Synelixis
- Evaluate the tool-chain on designer's productivity in the design and verification process
- Metrics: application speed, cost and power consumption

Expected results

- **20% productivity improvement** due to seamless implementation and verification of dynamically changing systems
- **50% total ownership cost reduction** for Network Intrusion Detection (NID) and Reverse Time Migration (RTM)
- **2x performance improvement** under power constraints for Global Illumination and Image Analysis

Project Details

Contract number
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Community contribution
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