FACILITATING ANALYSIS AND SYNTHESIS TECHNOLOGIES FOR EFFECTIVE RECONFIGURATION

Key innovation

Extending product functionality and lifetime requires constant addition of new features to satisfy the growing customer needs and the evolving market and technology trends. Software component adaptivity is straightforward but not enough: recent products include hardware accelerators – for reasons of performance and power efficiency – that also need to adapt to new requirements. For example, a Network Intrusion Detection System (NIDS) needs to scan all incoming network packets for suspicious content. The scanning has to be fast so that the monitored communication links are not slowed down, while the list of threats to check for is extended and updated on a daily basis.

Reconfigurable logic allows the definition of new functions to be implemented in dynamically instantiated hardware units, combining adaptivity with hardware speed and efficiency. For the Intrusion Detection System example, new rules can be hardcoded into the reconfigurable logic, achieving high performance, while providing the necessary adaptivity to new threats.

FASTER will facilitate the use of reconfigurable technology by providing a complete methodology that enables designers to easily implement and verify applications on platforms with general-purpose processors and acceleration modules implemented in the latest reconfigurable technology. We expect that the project will lead to a 20% productivity improvement due to seamless implementation and verification of dynamically changing systems, a 50% total ownership cost reduction for NIDS and Reverse Time Migration systems, with a 2x performance improvement under power constraints for Global Illumination and Image Analysis.

Technical approach

The FASTER tool-chain input will be based on hardware description languages or high-level programming languages with an initial decomposition described using existing formalisms (such as OpenMP). This input will be transformed to the corresponding task graph, which in turn will be partitioned in space and time using new algorithms derived from graph theory. We will pursue a task-cluster definition of a system specification by detecting recurrent structures in the specification, and consider them as candidates for reconfiguration. FASTER will support both region- and micro-reconfiguration (a technique that reconfigures very small parts of the device), an ability that opens up a new range of application opportunities for run-time reconfiguration.

FASTER will develop novel techniques for optimizing and verifying static and dynamic aspects of a reconfigurable design, while minimizing run-time overheads on speed, area and power consumption. FASTER will also provide a powerful run-time system that will be able to run on multiple reconfigurable platforms and manage the various aspects of parallelism and adaptivity with reduced overhead.

Contract number

287804

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FORTH-ICS

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Project website

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Community contribution to the project

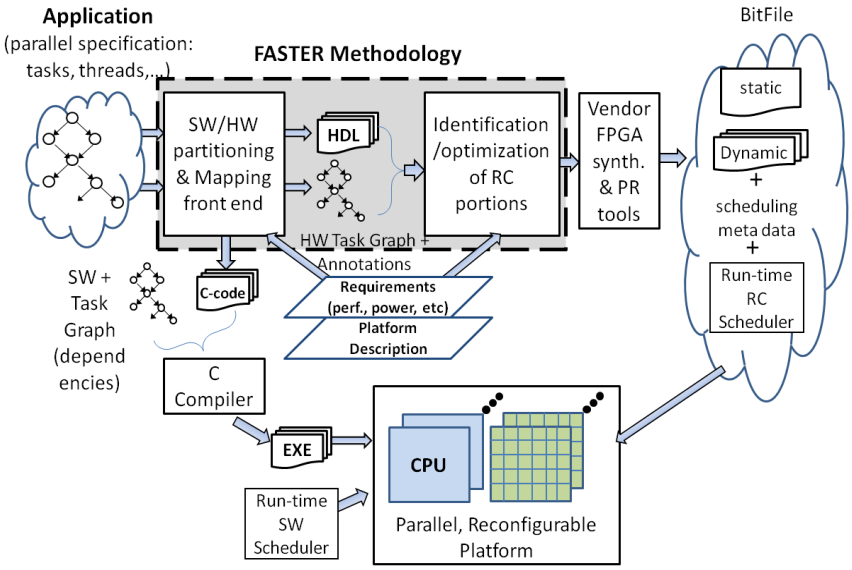
2.8 M€

Project start date

September 1st, 2011

Duration

36 months



Demonstration and Use

To demonstrate the effectiveness of the FASTER tool-chain, we will use three complex applications from different application domains: (a) Reverse Time Migration (RTM), a computational seismography algorithm, (b) Global Illumination and Image Analysis, and (c) a Network Intrusion Detection System (NIDS). We will evaluate the effect of the FASTER tool flow on designer productivity in the design and verification process. We will also use prototype platforms to evaluate the speed, cost, and power consumption of the applications implemented within FASTER.

Scientific, Economic and Societal Impact

The participation of ST Microelectronics, the world's fifth largest semiconductor company, and of Maxeler and Synelixis, two high-potential SMEs, ensures that the FASTER tool flow will be designed, tested and evaluated in close collaboration with the engineers that will eventually use it. The results of the project will strengthen the competitiveness of the industrial project partners as they will be able to deploy advanced market solutions with improved cost/performance and, thanks to adaptivity, with extended lifetime. The academic project partners will disseminate project results within their educational and research programs and in high-impact conferences and journals, advancing European excellence in education and research.

Project partners	Country
FORTH-ICS	Greece
Chalmers	Sweden
Imperial College London	United Kingdom
Politecnico di Milano	Italy
Gent University	Belgium
Maxeler	United Kingdom
ST Microelectronics	Italy
Synelixis	Greece

Key Features

- 20% productivity improvement due to seamless implementation and verification of dynamically changing systems
- 50% total ownership cost reduction for Network Intrusion Detection Systems and Reverse Time Migration
- 2x performance improvement under power constraints for Global Illumination and Image Analysis