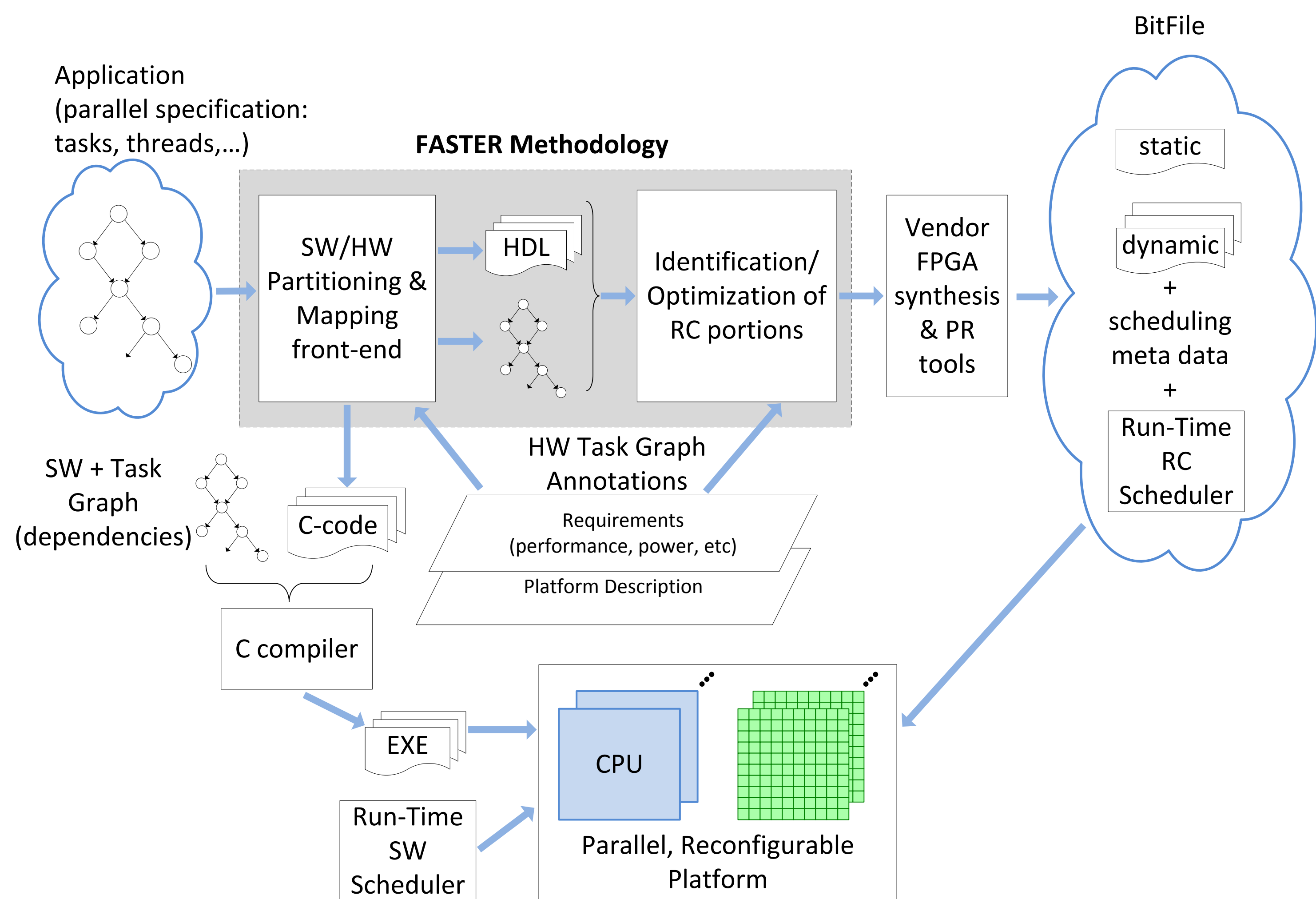


1) The FASTER Project

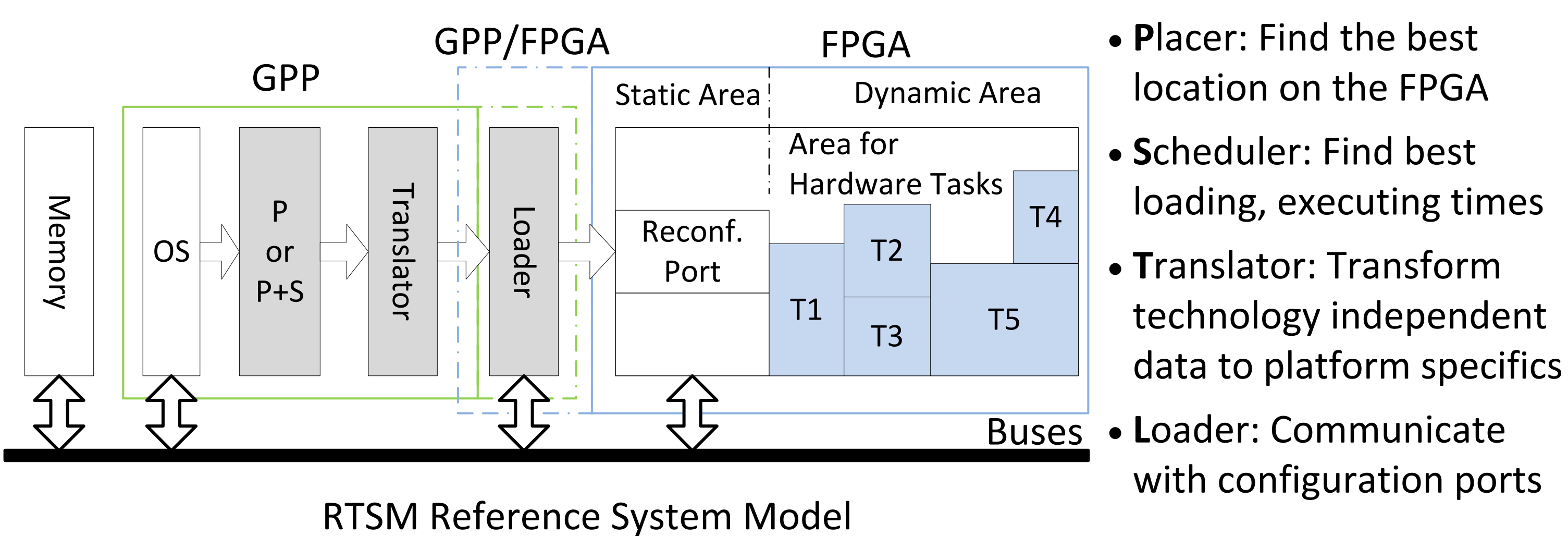
Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration
Goal: Reducing the complexity of Dynamic Partial Reconfiguration



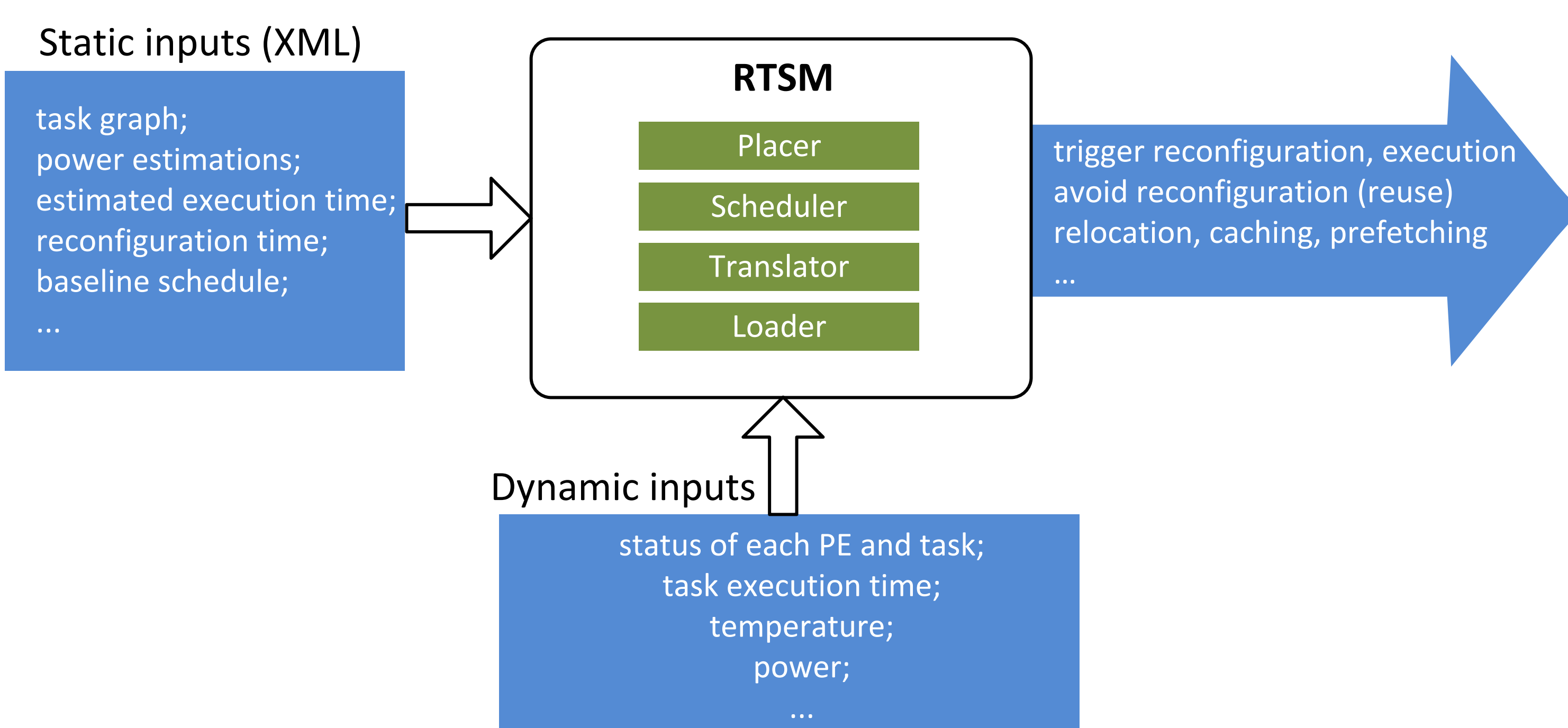
Primarily focused on **partial dynamic reconfiguration** with two options:
 a) **Region-based:** large device portions, precompiled circuits
 b) **Micro-reconfiguration:** small circuits specialized at runtime based on dynamic inputs

2) Run-Time System Manager (RTSM)

Low-level **scheduling and resource management** decisions



3) RTSM Functionality

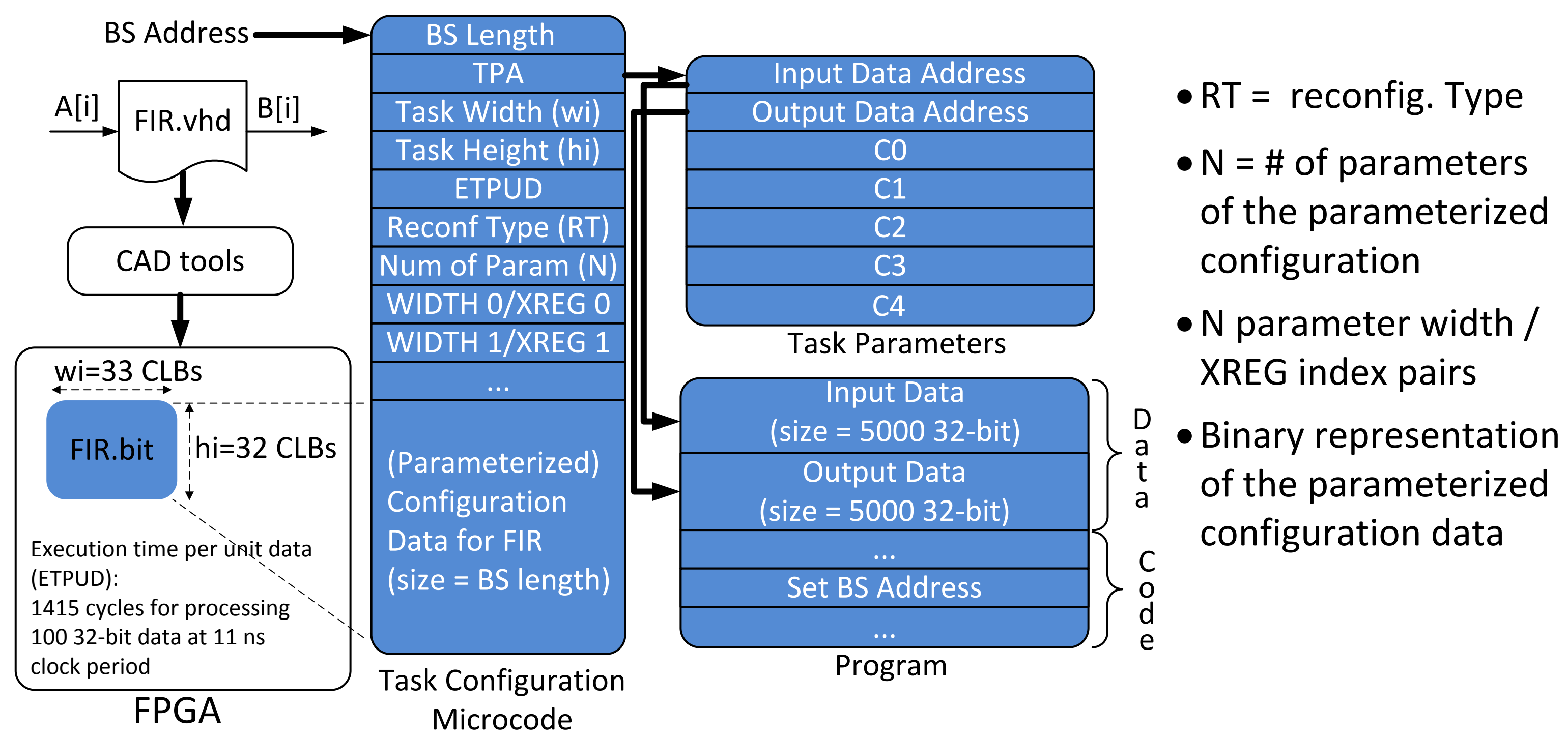


RTSM fed with **static** and **dynamic** inputs
 • **static:** from XML with scheduling alternatives to reconfigure the FPGA
 • **dynamic:** updated with FPGA runtime status



4) RTSM Architectural Interface

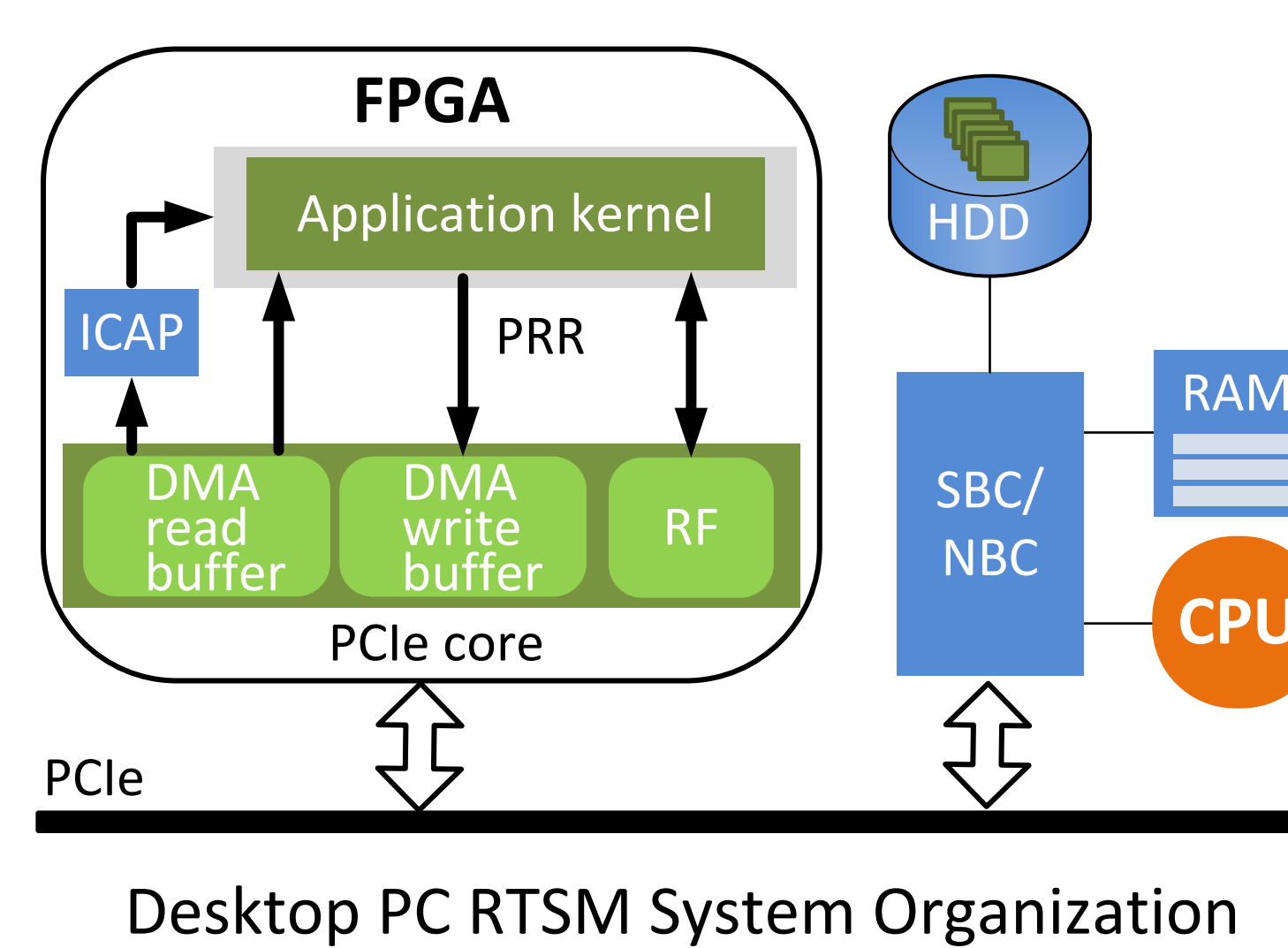
Technology Independent Bitstream Format with **Micro reconfiguration support**



Configuration agnostic ISA extension with:

- Full support for loosely coupled accelerators
- Support for micro-reconfiguration and for two level nested region/micro-reconfiguration
- Reconfiguration in 2 **logical** phases "SET EXECUTE address"
- Total of 5 new instructions: **P-SET, C-SET, EXECUTE, BREAK, SET PREFETCH**
- **Native Partial Reconfiguration Support**
 - **P-SET** (partial set): configure common parts of multiple (frequently used) functions
 - **C-SET** (complete set): configure the remaining blocks (not covered by P-SET) to complete the functionality
- Support for bitstream **prefetching:** SET PRFETCH

5) RTSM Prototype



RTSM prototyped on a desktop PC with:

- Intel Core i7-950, 3.06GHz
- CentOS Linux 6.4 64-bit
- 6GB DDR3@1600MHz
- One reconfigurable area
- Host CPU controls FPGA reconfiguration
- Bitstreams stored in HDD
- Bitstreams cached in host RAM

6) Results and Future Directions

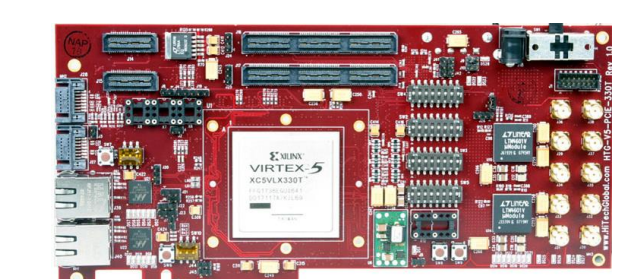
A) Xilinx University Program XUPV5

Virtex 5-LX110T
 Two XCF32P Platform Flash PROMs 32MB each
 256MB DDR2
 PCIe v1 x1, 2Gbps bandwidth



B) HiTechGlobal HTG-V5-PCIE-330

Virtex 5-LX330T
 4 MB Flash Memory
 2 GB DDR2
 PCIe v1 x4, 8Gbps bandwidth



	XUPV5 on PCIe v1 (x1)	HTG-V5 on PCIe v1 (x4)
	A)	B)
Transfer Rate	1.5 Gbps	4 Gbps
Reconfiguration Rate	0.8 Gbps	3.5 Gbps

Results show that the transition to faster PCIe mitigated the PCIe bottleneck

- Increased transfer by 2.7 times (CPU ↔ FPGA)
- Increased reconfiguration rate by 4.4 times (CPU → ρ FPGA)

Future (ongoing) work: Maxeler MaxWorkstation

Max3 dataflow engine
 Virtex 6 SX475T FPGA, 24GB memory
 Intel i7 2600s@2.8GHz, 16GB RAM

